课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	**课程名称 Course Title**	片上系统集成电路设计 System-on-a-Chip Design
2.	**授课院系** **Originating Department**	深港微电子学院 School of Microelectronics
3.	**课程编号** **Course Code**	SME317
4.	**课程学分 Credit Value**	3
5.	**课程类别** **Course Type**	专业选修课 Major Elective Courses
6.	**授课学期** **Semester**	秋季 Fall
7.	**授课语言** **Teaching Language**	中英双语 English & Chinese
8.	**授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师）** **Instructor(s), Affiliation& Contact** **（For team teaching, please list all instructors）**	Fengwei An School of Microelectronics anfw@sustech.edu.cn 安丰伟 深港微电子学院
9.	**实验员/助教、所属学系、联系方式** **Tutor/TA(s), Contact**	待公布 To be announced
10.	**选课人数限额(可不填)** **Maximum Enrolment（Optional）**	

11. 授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
学时数 Credit Hours	26	2	32	4 (Presentations)	64

12. 先修课程、其它学习要求 Pre-requisites or Other Academic Requirements	EE202 数字电路
13. 后续课程、其它学习规划 Courses for which this course is a pre-requisite	
14. 其它要求修读本课程的学系 Cross-listing Dept.	

教学大纲及教学日历 SYLLABUS

15. 教学目标 Course Objectives

To learn the RISC CPUs and SoC with these RISC CPUs

学习常用的精简指令集处理器和基于这些处理器的片上系统

To learn the bus interconnections in SoCs

学习各种片上系统的总线协议

To learn how to use EDA tools to simulate, synthesize, and place & route a design

学习如何使用 EDA 工具仿真、综合、布局布线一个电路设计

To learn how to design a simple IP core for SoCs

学习如何设计一个简单的 IP 核

16. 预达学习成果 Learning Outcomes

Have a high-level understanding of RISC CPUs and SoCs with these RISC CPUs

了解精简指令集处理器和基于精简指令集处理器的片上系统

Be capable to read data sheets and manuals

可以读懂技术说明书

Be capable of using EDA software to simulate, synthesize and map the RTL design

可以用常用的 EDA 工具仿真、综合、布局布线一个 RTL 设计

Have a high-level understanding of Intellectual property, reuse, and verification issues.

了解 IP 核的复用和验证

Be capable of doing RTL designs as a simple IP core for an SoC

可以用硬件设计语言设计一个简单的 IP 核

Be capable to present their own ideas

可以讲解自己的想法

17. 课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）
Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

Introduction to SoC 片上系统背景介绍 （2 hours）

SoC CPU cores 常用嵌入式 CPU 核（10 hours）

A. MIPS
B. ARM
C. RISC V
D. NIOS II
E. MicroBlaze

SoC interconnections 片上系统内部总线协议 （4 hours）

A. AMBA
B. WishBone/Avalon

Embedded system & real-time operating system 嵌入式系统及实时操作系统 （1 hours）

Hardware/Software co-design 硬件软件协同（1 hours）

SoPC (System on Programmable chips) 在可重构设备上的片上系统（1 hours）

Case study: Image Signal Processing (ISP) SoC design 实例：图像信号片上系统（ 7 hours）

A. System specification
B. Algorithm definition
C. RTL design
D. Synthesis
E. Place & Route
F. Validation and measurement
G. Implementation on FPGA

Third-party peripherals and IP cores reuse 第三方外设以及其他核的复用（2 hours）

Tutorials 习题辅导 (2 hours)

Presentations 演讲报告 (4 hours)

Labs: Algorithms and RTL design 算法建模和 RTL 体系结构设计 (4 hours)

Labs: Behavior simulation 仿真 (4 hours)

Labs: Synthesis and verification 综合与验证(4 hours)

Labs: post-simulation and post-timing analysis 后仿真与时序分析(4 hours)

Labs: Place and Route (IC compiler) 布局布线 (4 hours)

Labs: Validation (DRC LVS by Caliber) 物理验证(4 hours)

Labs: Implementation on FPGA 基于 FPGA 的实现(4 hours)

Labs: Projects (IP design for SoC on an FPGA) 基于 FPGA 的片上系统实现(4 hours)

18. 教材及其它参考资料 Textbook and Supplementary Readings

Textbooks:

P. Marwedel, Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems, 2nd edition, Springer, 2011

D. Harris, S. Harris, Digital Design and Computer Architecture, Second Edition, Elsevier, 2012.

R. C. Gonzalez, R. E. Woods, Digital Image Processing, Second Edition, Prentice Hall, 2001

课程评估 ASSESSMENT

19.

评估形式 Type of Assessment	评估时间 Time	占考试总成绩百分比 % of final score	违纪处罚 Penalty	备注 Notes
出勤 Attendance		10		
课堂表现 Class Performance				
小测验 Quiz				
课程项目 Projects		20		
平时作业 Assignments				
期中考试 Mid-Term Test		30		
期末考试 Final Exam		30		
期末报告 Final Presentation		10		
其它（可根据需要改写以上评估方式） Others (The above may be				

modified as necessary)				

20. 记分方式 **GRADING SYSTEM**

■ A. 十三级等级制 **Letter Grading** ☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

课程审批 REVIEW AND APPROVAL

21. **本课程设置已经过以下责任人/委员会审议通过**
This Course has been approved by the following person or committee of authority
