课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	**课程名称 Course Title**	集成电路版图设计基础 The Foundation of IC Layout Design
2.	**授课院系 Originating Department**	深港微电子学院 School of Microelectronics
3.	**课程编号 Course Code**	SME311
4.	**课程学分 Credit Value**	1
5.	**课程类别 Course Type**	专业选修课 Major Elective Courses
6.	**授课学期 Semester**	秋季 Fall
7.	**授课语言 Teaching Language**	中英双语 English & Chinese
8.	**授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师） Instructor(s), Affiliation& Contact （For team teaching, please list all instructors）**	蒋苓利，教学工程师，深港微电子学院，jiangll@sustech.edu.cn Lingli Jiang, Teaching engineer, School of Microelectronics, jiangll@sustech.edu.cn
9.	**实验员/助教、所属学系、联系方式 Tutor/TA(s), Contact**	待公布 To be announced
10.	**选课人数限额(可不填) Maximum Enrolment （Optional）**	

11.	授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
	学时数 Credit Hours	0	0	32	0	32

12.	先修课程、其它学习要求 Pre-requisites or Other Academic Requirements	SME306 先进数字 CMOS 集成电路设计 Advanced Digital CMOS IC Design 或 SME307 CMOS 模拟集成电路设计 CMOS Analog Integrated Circuit Design
13.	后续课程、其它学习规划 Courses for which this course is a pre-requisite	No
14.	其它要求修读本课程的学系 Cross-listing Dept.	No

教学大纲及教学日历 SYLLABUS

15. 教学目标 Course Objectives

集成电路版图设计将集成电路设计和工艺制造链接成一个整体。本课程的教学目标在于学习集成电路的版图设计，上下连接并融会贯通集成电路设计及基本制造工艺。

本课程将进行以下知识的学习：

1. 版图与器件剖面结构的对应关系；
2. 集成电路设计涉及的基本 CMOS 器件的版图设计，包括：无源器件、二极管、双极型晶体管、场效应晶体管；
3. 集成电路版图设计软件的使用；
4. 模拟集成电路绘制的基本原则，包括匹配原则、噪声原则等；
5. 子电路模块的绘制原则。

Integrated circuit layout design links IC design and process manufacturing into a whole. The teaching goal of this course is to learn the layout design of integrated circuits.The following knowledge will be learned in this course:

1. The corresponding relationship between layout and device profile structure;
2. The layout design of basic CMOS devices involved in IC design, includes: passive devices, diodes, bipolar transistors and field effect transistors.
3. The IC layout design software operation;
4. The basic principles of analog integrated circuit drawing, including matching principle, noise principle, etc.
5. Route principle of sub-circuit.

16. 预达学习成果 Learning Outcomes

通过本课程的学习，学生应当掌握以下知识：

1. 能看懂工艺厂商提供的规则文件；
2. 对于常规 CMOS 工艺器件，能根据版图文件画出对应的剖面结构；
3. 能根据给定的规则文件，设计常规的器件版图；
4. 能根据给定的工艺 PDK 文件和子电路文件，设计模拟集成电路版图；
5. 模拟电路版图设计中，能对面积、匹配、噪声等因素进行综合考虑。

Through this course, students should master the following knowledge:

1. Understand the rule files provided by the manufacturer;

2. For conventional CMOS devices, the corresponding section structure can be obtained according to the layout file.

3. Can design conventional device layout according to the given rule files;

4. The layout of analog integrated circuits can be designed according to the given process PDK files and sub-circuit files.

5. In the layout design of analog circuits, area, matching, noise and other factors can be considered comprehensively.

17. 课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）
Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

1-4 学时：Cadence 软件中 virtuoso 工具的操作方法。

5-8 学时：学习基本 CMOS 工艺流程中版图与工艺的对应关系，从而理解由版图还原器件剖面结构的基本原理，学会如何分析还原器件结构。

9-12 学时：CMOS 工艺中基本元器件学习，学会根据设计规则绘制基本元器件；

13-16 学时：分析和学习模拟集成电路中匹配的相关知识，学会哪些电路单元需要进行匹配，学会如何进行匹配。

17-20 学时：分析和学习模拟集成电路中噪声的相关知识，学会哪些电路单元需要进行噪声屏蔽处理，学会如何进行噪声屏蔽处理。

21-32 学时：提供 PDK 及模拟集成电路子电路，指导学生进行版图绘制。此为设计实战演练，约需 12 小时时间完成。学生在完成后，需向全班同学讲述本人绘制版图的思路和各细节处理方式，并进行集体点评。

1-4 hours: The operation of Virtuoso tool in Cadence software.

5-8 hours: Learn the relationship between layout and process in basic CMOS process flow, and learn how to obtain the profile structure from the layout file.

9-12 hours: Learning basic components in CMOS process and learning to draw basic components according to design rules

13-16 hours: Learn the knowledge of match in analog integrated circuits, learn which circuit units need match, and learn how to deal with match in layout design.

17-20 hours: Learn the knowledge of noise in analog integrated circuits, learn which circuit units need noise shielding, and learn how to deal with noise shielding..

21-32 hours: According to the PDK and analog integrated circuit provided, guide students to design the layout. It takes about 12 hours to complete the design exercise. After completion, the students need to explain their ideas and details of the layout, and make a collective comment

18. 教材及其它参考资料 Textbook and Supplementary Readings

The Art of Analog Layout，Alan Hastings， 电子工业出版社，第 2 版，ISBN： 9787121367526

课程评估 ASSESSMENT

19.	评估形式 Type of Assessment	评估时间 Time	占考试总成绩百分比 % of final score	违纪处罚 Penalty	备注 Notes
	出勤 Attendance				
	课堂表现 Class Performance		10%		
	小测验 Quiz				
	课程项目 Projects		90%		
	平时作业 Assignments				
	期中考试 Mid-Term Test				
	期末考试 Final Exam				
	期末报告 Final Presentation				
	其它（可根据需要改写以上评估方式） Others (The above may be modified as necessary)				

20. 记分方式 GRADING SYSTEM

☑ A. 十三级等级制 Letter Grading
☐ B. 二级记分制（通过/不通过） Pass/Fail Grading

课程审批 REVIEW AND APPROVAL

21. 本课程设置已经过以下责任人/委员会审议通过
This Course has been approved by the following person or committee of authority