南方科技大学 SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	**课程名称 Course Title**	**集成电路前沿-微处理器设计** **Advanced Integrated Circuit Design: Microprocessor**
2.	**授课院系** **Originating Department**	电子与电气工程系 Department of Electrical and Electronic Engineering (EEE)
3.	**课程编号** **Course Code**	EE341
4.	**课程学分 Credit Value**	3
5.	**课程类别** **Course Type**	专业选修课 Major Elective Courses
6.	**授课学期** **Semester**	秋季 Fall
7.	**授课语言** **Teaching Language**	中英双语 Chinese and English
8.	**授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师）** **Instructor(s), Affiliation& Contact** **（For team teaching, please list all instructors）**	余浩(副教授)， 电子与电气工程系 办公室：第一教学楼 104 室 邮箱：yuh3@sustc.edu.cn 电话：0755-8801-8575 YU, Hao, Assoc. Prof., Department of Electrical and Electronic Engineering Office: Room 104, Teaching Building 1 Email: yuh3@sustc.edu.cn Telephone: 0755-8801-8575
9.	**实验员/助教、所属学系、联系方式** **Tutor/TA(s), Contact**	董龙涛、刘斌， 硕士生，电子与电气工程系 邮箱：donglt@mail.sustc.edu.cn 电话：15039586999
10.	**选课人数限额(可不填)** **Maximum Enrolment（Optional）**	

11. 授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
学时数 Credit Hours	32	0	32		64

12. 先修课程、其它学习要求 Pre-requisites or Other Academic Requirements	EE202-17 数字电路 EE202-17 Digital circuit
13. 后续课程、其它学习规划 Courses for which this course is a pre-requisite	本课程为电子与电气工程系微电子专业选修课，主要计算机体系结构及硬件实现与应用。其它专业学生如果想学习相关知识也可选修本课程。 This course is the elected course for undergraduate student in Microelectronics, and it includes the basic architecture theory, hardware implementation and application microprocessor. It should however also be suitable for non-specialists, i.e. for all those students who show interests in lasers to gain a certain amount of relevant knowledge.
14. 其它要求修读本课程的学系 Cross-listing Dept.	无 None

教学大纲及教学日历 SYLLABUS

15. 教学目标 Course Objectives

本课程旨在培养本科生在数字电路芯片设计的兴趣与能力。本课程分为三个部分：1. 计算机架构理论的学习；2. 了解计算单元设计及存储设计要点；3. 对上述理论模型进行硬件实现。

After the completion of this course, students should know the following items. (1) Familiar with the basic theory of machine learning algorithms (2) Utilize software platforms to train and verify the machine learning algorithms and models, including classification and clustering (3) Implement the machine learning models on hardware by Verilog.

16. 预达学习成果 Learning Outcomes

本课是微电子专业的主干专业课，致力于让学生们了解芯片与微处理器设计所面临的核心技术难题，通过培养学生理论与动手能力深入探索新架构、新器件和新电路， 通过开设基于微处理器 RISC-V 指令集机构的软件平台，学会并培养分析解决微处理器与嵌入式系统问题的能力，并将算法实现在硬件中，为今后从事芯片设计科研及开发工作打下良好的专业基础。

This course is the core course for students in Microelectronics. This course will focus on teach the students understand the core challenge in IC and microchip design, as well as with the theory and experiment the students will deeply understands the state of arts CPU devices. Based on the RISC-V hardware and software platform training, the students will also achieve the ability of analysis and solve the problem in microchip and embedded system. It is essential for students to engage in research and development of microprocessor design, artificial intelligence and integrated circuit design in the future.

17. **课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）**
Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

Lecture（授课）
Week 1 to 3: Introduction of IC design and scaling； Introduction of microprocessor design (6hrs)
集成电路设计导论；微处理器设计导论；

Week 4 to 6: Lecture on various processor microarchitecture, including parallel design method, pipelined design method, and according modern design specs (low power and high throughput) (6hrs)
微处理器架构；并行架构；流水线架构；现代处理器设计指南（低功耗高通量）

Week 7 to 9: Lecture on various memory microarchitecture, including SRAM and DRAM, memory hierarchy, memory access model, cache design, memory bank design and emerging memory (6hrs)
存储器架构；静态动态存储器; 存储结构；内存访问模型；存储阵列设计；新型非易失存储器；

Week 9 to 12: Mid-term quiz; Lecture on RISC-V instruction set； embedded system designs with ARM core and also design of machine learning chip (8hrs)
期中考核；RISC-V 指令集；嵌入式系统和 ARM 核；机器学习架构；

Week 13-16: Lecture on Verilog design on hardware platform (6hrs)
基于 Verilog 的硬件语言及实现；

Experiment（实验）
Experiment of hardware implementation for microprocessor. Students are required to implement one of simple pipelined microprocessor on a hardware platform (RISC-V). Students will do this project in groups of 2-3. Students need to have a presentation and submit a report for evaluation of this project.
实验课程实现微处理器芯片设计；实现简单的 RISC-V 的流水线处理器；2-3 人一组；交付实验报告及口头演示；

Week 1-4 VLSI Tool flow (8hrs)
(a) obtain working RTL checked into your private git repository at Github (2hrs)
(b) build results and reports generated by VCS, DC Compiler, Formality, IC Compiler, and PrimeTime PX checked into your git repo (results and reports only!) (2hrs)
(c) written answers to the questions given at the end of this document checked into repository as writeup/report.pdf or writeup/report.txt (4hrs)
大规模集成电路设计流程实验及调试：RTL 代码的 VLSI 流程实现，测试及报告

Week 5-8 Experimental study of RISC-V basics (8hrs)
(a) C source code and assembly code checked into your git report (2hrs)
(b) Python scripts to parse simulation results and power reports (2hrs)
(c) build results for DC, ICC, and Primetime (4hrs)
RISC-V 指令集学习实验调试；

Week 9-12 Experimental study of Accelerator (8hrs)
(a) your working Chisel RTL checked into your private git repository at Github (2hrs)
(b) Reports (only!) generated by DC Compiler, IC Compiler, and PrimeTime PX checked into your git repo for the three implementations of your design (2hrs)
(c) written answers to the questions given at the end of this document checked into your git repository as writeup/lab3-report.pdf or writeup/lab3-report.txt (4hrs)
卷积加速器设计；

Week 13-16 Experimental implementation of RISC-V (8 hours)

(a) your working Chisel RTL checked into your private git repository at Github (2hrs)
(b) Reports (only!) generated by DC Compiler, IC Compiler, and PrimeTime PX checked into your git report (2hrs)
(c) working C code for matrix sum (2hrs)
(d) written answers to the questions given at the end of this document checked into your git repository as writeup/lab4-report.pdf or writeup/lab4-report.txt (2hrs)
加速器与 RISC-V 集成

18. **教材及其它参考资料 Textbook and Supplementary Readings**

Computer architecture a quantitative approach

[John L. Hennessy, David A. Patterson]

课程评估 ASSESSMENT

19.

评估形式 Type of Assessment	评估时间 Time	占考试总成绩百分比 % of final score	违纪处罚 Penalty	备注 Notes
出勤 Attendance		10		
课堂表现 Class Performance		10		
小测验 Quiz		0		
课程项目 Projects		0		
平时作业 Assignments		30		
期中考试 Mid-Term Test		20		
期末考试 Final Exam		30		
期末报告 Final Presentation				

其它（可根据需要改写以上评估方式） **Others (The above may be modified as necessary)**				

20. 记分方式 **GRADING SYSTEM**

✓ A. 十三级等级制 **Letter Grading** ☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

课程审批 REVIEW AND APPROVAL

21. 本课程设置已经过以下责任人/委员会审议通过
This Course has been approved by the following person or committee of authority
