南方科技大学 SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	课程名称 Course Title	数字系统设计 Digital System Design
2.	授课院系 Originating Department	电子与电气工程系 Department of Electrical and Electronic Engineering
3.	课程编号 Course Code	EE332
4.	课程学分 Credit Value	3
5.	课程类别 Course Type	专业核心课 Major Core Courses 专业选修课 Major Elective Courses
6.	授课学期 Semester	春季 Spring
7.	授课语言 Teaching Language	英文 English
8.	授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师） Instructor(s), Affiliation& Contact （For team teaching, please list all instructors）	虞亚军，副教授，电子与电气工程系 Associate Professor YU Yajun, Department of Electrical & Electronic Engineering Email: yuyj@sustech.edu.cn Tel: 0755-88018557
9.	实验员/助教、所属学系、联系方式 Tutor/TA(s), Contact	待公布 To be announced
10.	选课人数限额(可不填) Maximum Enrolment （Optional）	50

11. 授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
学时数 Credit Hours	32		32		64

12.	先修课程、其它学习要求 **Pre-requisites or Other Academic Requirements**	EE202-17 数字电路 Digital Electronics
13.	后续课程、其它学习规划 **Courses for which this course is a pre-requisite**	
14.	其它要求修读本课程的学系 **Cross-listing Dept.**	

教学大纲及教学日历 SYLLABUS

15. **教学目标 Course Objectives**

本课程介绍了一种用于对数字逻辑系统进行描述，仿真，综合，实现的硬件描述语言(HDL)。学生通过大量的实验，使用电子设计自动化工具来设计和实现数字逻辑系统。

The objective of this course is to introduce a hardware description language (HDL) for the specification, simulation, synthesis and implementation of digital logic systems. The students will have design practice sessions designing and implementing digital logic systems with commercial electronic design automation (EDA) tools.

16. **预达学习成果 Learning Outcomes**

通过这门课程的学习，学生能够
1. 掌握硬件描述语言 VHDL，并用 VHDL 对数字系统进行归档，仿真和综合；
2. 理解数字系统涉及到方法，以及性能，价格的指标：
3. 运用 VHDL，设计数字系统以实现特定功能，平衡性能价格比；
4. 熟练掌握数字系统设计的开发环境 Vivado；以及
5. 设计和实现数字系统以解决实际问题。

After completing this course, students are able to
1. Master a hardware description language VHDL, and use VHDL to document, simulate and synthesis digital systems;
2. Understand the methodology, and the performance/cost criteria of digital system design,
3. Design a digital system to realize the specified functions, and trade-off between the performance and cost, using the VHDL;
4. Be skilful in using digital system development environment Vivado.
5. Design and implement digital system to solve real problems.

17. **课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）**
Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

Digital Design using Hardware Description Language (32 hrs)

Design methodology. Levels of abstraction. VHDL syntax. Entity. Architecture. Types and objects. Operators and expressions. Concurrent statements. Sequential statements. Subprograms. Packages. Libraries. Behavioral, dataflow and structural coding styles. Test benches. Pipeline design. Parameterized design. Architectures and characteristics of CPLDs or FPGAs

Design Practice Module (16 hrs)

HDL design entry. Test benches for the design. Compilation and functional simulation. Fitting and placement of design into a CPLD or FPGA device. Timing simulation. Programming the design into a CPLD or FPGA device. Bench testing.

Project (16 hrs)

Students are required to design a digital system by using VHDL and implement the design into FPGA Sexys4-DDR.

18. 教材及其它参考资料 Textbook and Supplementary Readings

主要教材/text book：
RTL hardware design using VHDL, coding for efficiency, portability and scalability, by Pong P. Chu, Wiley-interscience

参考资料/references：
VHDL A Starter's Guide，作者 Sudhakar Yalamanchili, Pearson。
Digital System Design with VHDL， by Charles H. Roth, Jr., Lizy Kurian John，电子工业出版社。

课程评估 ASSESSMENT

19.

评估形式 Type of Assessment	评估时间 Time	占考试总成绩百分比 % of final score	违纪处罚 Penalty	备注 Notes
出勤 Attendance				
课堂表现 Class Performance				
小测验 Quiz				
课程项目 Projects		30		
平时作业 Assignments		30		
期中考试 Mid-Term Test				
期末考试 Final Exam		40		
期末报告 Final Presentation				

其它（可根据需要改写以上评估方式） **Others (The above may be modified as necessary)**				

20. 记分方式 **GRADING SYSTEM**

☒ A. 十三级等级制 **Letter Grading**
☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

课程审批 REVIEW AND APPROVAL

21. 本课程设置已经过以下责任人/委员会审议通过
This Course has been approved by the following person or committee of authority