南方科技大学 SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	课程名称 Course Title	**数字逻辑 Digital Logic**
2.	授课院系 Originating Department	计算机科学与工程系 Department of Computer Science and Technology
3.	课程编号 Course Code	CS207
4.	课程学分 Credit Value	3
5.	课程类别 Course Type	专业基础课 Major Foundational Courses
6.	授课学期 Semester	秋季 Fall 春季 Spring
7.	授课语言 Teaching Language	英文 English
8.	授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师） Instructor(s), Affiliation& Contact （For team teaching, please list all instructors）	Georgios Theodoropoulos，讲席教授，计算机科学与工程系，georgios@sustech.edu.cn Georgios Theodoropoulos, Chair Professor, Department of Computer Science and Technology, georgios@sustech.edu.cn 余剑峤，助理教授，计算机科学与工程系，yujq3@sustech.edu.cn Jianqiao Yu, Assistant Professor, Department of Computer Science and Technology, yujq3@sustech.edu.cn
9.	实验员/助教、所属学系、联系方式 Tutor/TA(s), Contact	王薇，教学实验员，计算机科学与工程系，wangw6@sustech.edu.cn Wei Wang, Teaching laboratory technician, Department of Computer Science and Technology, wangw6@sustech.edu.cn
10.	选课人数限额(可不填) Maximum Enrolment （Optional）	

11. 授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
学时数 Credit Hours	32		32		64

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12.	先修课程、其它学习要求 **Pre-requisites or Other Academic Requirements**	无 NA
13.	后续课程、其它学习规划 **Courses for which this course is a pre-requisite**	无 NA
14.	其它要求修读本课程的学系 **Cross-listing Dept.**	无 NA

教学大纲及教学日历 SYLLABUS

15. 教学目标 Course Objectives

本课程为数字设计方面的基础课程，主要介绍数字设计基础概念、数字电路设计以及数字设计的主流方式及技术。数字逻辑是一种将电子电路中的信号和序列通过数字方式进行表达的科学方法，是数字运算的基础。学生通过学习数字逻辑从本源上理解现代电子计算机中电路与硬件的沟通方式。数字逻辑以嵌入式逻辑的方式广泛应用于大量电子设备，包括计算器、计算机、手表等。虽然大多数现代逻辑设计是通过计算机方法完成，本课程涵盖了这些计算机辅助设计方法的基本构建原理和构建方法。本课程介绍核心逻辑运算，并展示为实现特定逻辑功能设计逻辑电路的基本方法。本课程同时介绍组合电路及同步时序电路的基本原理及其在计算设备中的高级应用组成方式。本课程通过使用算法和简单输入的方式使学生获得第一手构建计算机硬件的经验。学生将会学习如何通过二元输入在计算机中存储文档、图片、声音及视频等类信息并对其进行逻辑处理。本课程将传授给学生数字设计中的基础概念、问题、数字设计的工程准则，以及组合及时序电路的设计方法。同时，本课程为学生提供通过硬件描述语言进行实际数字硬件设计的经验。

This is a foundational course in digital design that aims to provide an understanding of the fundamental concepts, circuits in digital design, and expose students to the mainstream approaches and technologies used in digital design. Digital logic is the representation of signals and sequences of a digital circuit through numbers. It is the basis for digital computing and provides a fundamental understanding on how circuits and hardware communicate within a computer. Digital logic is typically embedded into most electronic devices, including calculators, computers, and watches. This field is utilized by many careers that work with computers and technology. Although most modern logic design is now achieved with computerized methods, this course covers the essential building blocks upon which modern techniques were developed. This course introduces the core logical operations and demonstrates elementary methods to design logic circuits to achieve a desired function. This course also introduces the fundamentals of combinational and sequential circuits, with their high-level implementations as demonstrations. This course allows students to gain hands-on experience by building computer hardware through the use of algorithms and simple inputs. They learn how simple inputs of ones and zeros can be used to store information on computers, including documents, images, sounds, and videos. Students should be able to demonstrate an in-depth knowledge of the fundamental concepts and issues and the engineering principles involved in digital design and be able to design a series of combinational and sequential circuits. In addition, they should demonstrate through hands-on experimentation knowledge of the digital design process using HDLs.

16. 预达学习成果 Learning Outcomes

在课程完成时，学生可获得以下技能：

- 理解与或非、与非、或非等基础逻辑操作、原理图符号和真值表；
- 使用卡诺图等方法优化布尔式及逻辑代数；
- 使用布尔式或真值表分析及设计组合电路及使用时序图分析及设计时序电路；
- 理解寄存器的设计原理、使用方法及工业设计准则；
- 理解如何应用所学数字逻辑概念实现完成实际逻辑运算需求。

On completion of this course, students should be able to

- Understand fundamental logic operations - e.g., AND, OR, NOT, NAND, NOR, etc. -, schematic symbols and diagrams, and truth tables;
- Optimize Boolean functions and algebra with Karnaugh maps method;
- Design combinational logic circuits with Boolean functions or truth tables, and design sequential logic circuits

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with timing diagrams;

- Understand the theory, usage, and design principle of registers;
- Understand how to implement practical logic functions with digital logic theory.

17. **课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）**
Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

- **Week 1: Course Introduction and Binary Numbers [2h lecture + 2h lab]**
  - Course overview and logistics
  - Binary, octal, hexadecimal numbers
  - Binary codes and basic binary logic
  - [Lab] Verilog introduction and basic operations
- **Week 2: Boolean Algebra and Logic Gates [2h lecture + 2h lab]**
  - Boolean function
  - Canonical and standard form function
  - Digital logic gates
  - [Lab] Verilog for boolean algebra
- **Week 3: Gate-Level Minimization - Part 1 [2h lecture + 2h lab]**
  - The Karnauph map simplification method
  - Three- and four-variable K-map
  - Prime implicants and don't care condition
  - [Lab] Operators and primitives
- **Week 4: Gate-Level Minimization - Part 2 [2h lecture + 2h lab]**
  - NAND and NOR implementation
  - Other two-level logic function implementation
  - XOR function implementation
  - [Lab] Behavioral modeling
- **Week 5: Combinational Logic - Part 1 [2h lecture + 2h lab]**
  - Combinational circuit
  - Analyze and design a combinational circuit
  - Half adder and full adder
  - [Lab] Task and function
- **Week 6: Combinational Logic - Part 2 [2h lecture + 2h lab]**
  - Binary adder and subtractor
  - Overflow and decimal adder
  - Binary multiplier and magnitude comparator

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  - [Lab] Combinational circuit
- **Week 7: Combinational Logic - Part 3 [2h lecture + 2h lab]**
  - Decoder and encoder
  - Combinational logic implementation
  - Multiplexer
  - [Lab] Decoder and encoder
- **Week 8: Synchronous Sequential Logic - Part 1 [2h lecture + 2h lab]**
  - Sequential circuits
  - Latches and flip-flops
  - Analysis of clocked sequential circuits
  - [Lab] Latches and flip-flops
- **Week 9: Synchronous Sequential Logic - Part 2 [2h lecture + 2h lab]**
  - State reduction
  - State assignment
  - Sequential circuit design procedure
  - [Lab] Design with sequential logic
- **Week 10: Registers and Counters - Part 1 [2h lecture + 2h lab]**
  - Registers
  - Shift registers
  - [Lab] Register design
- **Week 11: Registers and Counters - Part 2 [2h lecture + 2h lab]**
  - Ripple counters
  - Synchronous counters
  - Other counter types
  - [Lab] Counter design
- **Week 12: Memory and Programmable Logic - Part 1 [2h lecture + 2h lab]**
  - Random-access memory
  - Memory decoding
  - Error detection and correction
  - [Lab] Error detection and correction design
- **Week 13: Memory and Programmable Logic - Part 2 [2h lecture + 2h lab]**
  - Read-only memory
  - Programmable logic array
  - Programmable array logic
  - [Lab] Memory and logic design

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- **Week 14: Register Transfer Level Design - Part 1 [2h lecture + 2h lab]**
  - Register transfer level
  - Algorithmic state machines
  - ASMD chart
  - [Lab] Sequential register transfer level design
- **Week 15: Register Transfer Level Design - Part 2 [2h lecture + 2h lab]**
  - Control logic
  - Design with multiplexer
  - Race-free and latch-free design
  - [Lab] Sequential register transfer level design with principles
- **Week 16: Summary and Revision [2h lecture + 2h lab]**
  - [Lab] Summary and revision of logic design

18. 教材及其它参考资料 Textbook and Supplementary Readings

Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog (5th ed.), M. Morris Mano and Michael D. Ciletti

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课程评估 ASSESSMENT

19.

评估形式 Type of Assessment	评估时间 Time	占考试总成绩百分比 % of final score	违纪处罚 Penalty	备注 Notes
出勤 Attendance		10%		
课堂表现 Class Performance				
小测验 Quiz				
课程项目 Projects				
平时作业 Assignments		30%		数字逻辑理论和实验 Digital logic theory and experiment
期中考试 Mid-Term Test				
期末考试 Final Exam		60%		闭卷考试 Closed-book exam
期末报告 Final Presentation				

其它（可根据需要改写以上评估方式） **Others (The above may be modified as necessary)**				

20. 记分方式 **GRADING SYSTEM**

☑ A. 十三级等级制 **Letter Grading**
☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

课程审批 REVIEW AND APPROVAL

21. 本课程设置已经过以下责任人/委员会审议通过
This Course has been approved by the following person or committee of authority

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