课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	课程名称 Course Title	**计算机组成原理 Computer Organization Principle**
2.	授课院系 Originating Department	计算机科学与工程系 Department of Computer Science and Technology
3.	课程编号 Course Code	CS202
4.	课程学分 Credit Value	3
5.	课程类别 Course Type	专业基础课 Major Foundational Courses
6.	授课学期 Semester	春季 Spring
7.	授课语言 Teaching Language	英文 English 中英双语 English & Chinese
8.	授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师） Instructor(s), Affiliation& Contact （For team teaching, please list all instructors）	张进，助理教授，计算机科学与工程系，zhangj4@sustech.edu.cn Jin Zhang, Assistant Professor, Department of Computer Science and Technology, zhangj4@sustech.edu.cn ASHERALIEVA, Alia，助理教授，计算机科学与工程系，asheralievaa@sustech.edu.cn ASHERALIEVA, Alia, Assistant Professor, Department of Computer Science and Technology, asheralievaa@sustech.edu.cn
9.	实验员/助教、所属学系、联系方式 Tutor/TA(s), Contact	王薇，教学实验员，计算机科学与工程系，wangw6@sustech.edu.cn Wei Wang, Teaching laboratory technician, Department of Computer Science and Technology, wangw6@sustech.edu.cn
10.	选课人数限额(可不填) Maximum Enrolment （Optional）	

11. 授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
学时数 Credit Hours	32		32		64

12.	先修课程、其它学习要求 **Pre-requisites or Other Academic Requirements**	CS207 数字逻辑 Digital Logic
13.	后续课程、其它学习规划 **Courses for which this course is a pre-requisite**	无 None.
14.	其它要求修读本课程的学系 **Cross-listing Dept.**	无 Not applicable for other departments beside CS.

教学大纲及教学日历 SYLLABUS

15. 教学目标 Course Objectives

1.学习决定计算机系统性能的相关计算机系统的基本组成结构,理解计算机系统设计的基本设计思路和原理；

2.理解计算机体系结构与软件系统的相互关系；

3.了解现今各种计算机系统的系统架构和指令集架构。

1. Learning the organizational structures that determine the capabilities and performance of computer systems. Understanding the basic design principles of computer system.

2. Understanding the interactions between the computer's architecture and its software.

3. Review various computer systems and various instruction set of real computers nowadays.

16. 预达学习成果 Learning Outcomes

成功完成本课程后，学生将获得以下技能：

1.掌握计算机系统的基本概念、基本原理、基本设计和分析方法，主要包括指令集、CPU 的算术运算、流水线、层次存储结构以及并行计算机系统的基本原理和设计方法。

2.掌握基于 MIPS 指令集的汇编语言编程。

3.掌握基于 verilog 语言的 CPU 系统设计

4.理解计算机系统的硬件与软件的关联与依赖关系。

This course provides a solid theoretical foundation that furnishes the student with insight into the innermost workings of the modern digital computer, together with a thorough understanding of the organization and architecture of real computers. The main content students should grasp includes instruction set, arithmetic operation, pipeline, hierarchical memory and parallel processing.

Assembly language programing using MIPS instructions

Design a reduced CPU on a FPGA using Verilog.

Understand the interaction of hardware and software.

17. 课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）

Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

第一周 ：计算机组成原理导学：重要性, 计算机发展历史，对计算机的抽象理解

Lab 1. 学习 MIPS 仿真器 (QtSpim, Mars)的使用, 基于 MIPS 示例 程序加强练习

第二周：计算机系统性能

Lab 2. 编写基本的汇编程序，练习 load 与 store 指令以及基本的算术指令

第三周：ISA 指令及基本概念

Lab 3. 练习 MIPS 上的基本数据处理，包括大、小端，有符号数与无符号数，练习移位及逻辑运算指令

第四周：ISA 控制指令，过程的调用及返回

Lab 4. 练习分支及跳转指令，实现分支及循环处理

第五周：ISA 3：MIPS 寻址, 程序的处理及运行, C 语言实现排序, 其他流行的 ISA 介绍

Lab 5. 练习函数与宏的定义及调用, 练习堆与栈的处理

第六周：计算机中的算术运算 (整型数): 加减乘除及溢出处理

Lab 6. MIPS 中的异常处理, 练习如何设计及测试自定义的异常处理

第七周： 计算机中的算数运算 (浮点数): 加减乘除

Lab 7. 练习浮点数的处理

第八周：处理器: 逻辑设计的方法

Lab 8. MIPS 综合练习

第九周： 期中考试

Lab 9. vivido 软件及 minisys 开发板的使用,练习 verilog 实现模块及仿真

第十周： Pipeline 介绍：MIPS pipeline, pipeline 性能

Lab 10. 使用 verilog 创建一个 ALU

第十一周：指令级并行处理：调度示例, 循环及多态相关问题

Lab 11. 使用 verilog 实现控制单元

第十二周：层次化存储管理:SRAM, DRAM 以及 flash

Lab 12. 使用 verilog 实验地址译码

第十三周：Cache 访问及调用, 虚拟存储

Lab 13. 使用 verilog 实现存储及 IO 访问

第十四周：并行处理：SISD, MIMD, SIMD, SPMD and 向量机

Lab 14. 设计并实现支持简单 MIPS 指令的单周期 CPU (1)

第十五周：集群网络

Lab 15. 设计并实现支持简单 MIPS 指令的单周期 CPU (2)

第十六周：总结与复习

Lab 16. 复习与答疑

Lecture 1. Course introduction：

The importance of computer organization, background and computer abstraction

Lab 1. Practice on MIPS simulator (QtSpim, Mars), assembly and run a MIPS demo

Lecture 2. Computer System Performance

Lab 2. Practice on the load and store and arithmetic instruction.

Lecture 3. Instruction Set Architecture 1：

Instruction set architecture, instructions, basic concepts

Lab 3. Practice on the data process in MIPS, including big-endian and small-endian, signed and unsigned data, practice shift and logic instruction.

Lecture 4. Instruction Set Architecture 2：

Control instructions, procedure call/return

Lab 4. Practice on the branch and jump instruction, practice on switch and loop procession.

Lecture 5. Instruction Set Architecture 3：

MIPS addressing, translating and starting a program, a C sort example, other popular ISAs

Lab 5. Practice on the function and macro, practice the stack and heap

Lecture 6. Arithmetic for computers (Integers):

Addition and subtraction, multiple and division, dealing with overflow

Lab 6. Learn the exception in arithmetic operation, practice how to write a exception handler.

Lecture 7. Arithmetic for computers (floating point numbers):

Addition and subtraction, multiplication and division

Lab 7. Practice on the instruction on float-point data.

Lecture 8. Processor:

Methods for logical design

Lab 8. Using vivado and minisys to develop board, practice a verilog module.

Lecture 9. middle-examination:
Lab 9. practise on MIPS.

Lecture 10. Pipeline introduction:
MIPS pipeline, pipeline performance
Lab 10. Make an ALU by using Verilog.

Lecture 11. Instruction-level parallelism:
Scheduling example, loop unrolling, dynamic multiple issue,
Lab 11. Design the control unit by Verilog

Lecture 12. Memory Hierarchy:
SRAM, DRAM and flash
Lab 12. Design the decode unit by verilog.

Lecture 13. Cache access and invoking, virtual memory
Lab 13. Design a memory unit and I/O unit by Verilog.

Lecture 14. Parallel Processing:
SISD, MIMD, SIMD, SPMD and vector machine
Lab 14. Design a single cycle CPU which could process simple MIPS instruction (1)

Lecture 15. Cluster network
Lab 15. Design a single cycle CPU which could process simple MIPS instruction(continue)

Lecture 16. Summary & review
Lab 16. Review, Q&A

18. **教材及其它参考资料 Textbook and Supplementary Readings**

Computer Organization and Design – the HW/SW Interface, Patterson and Hennessy, 5th edition

Computer Architecture - a quantitative approach, Hennessy and Patterson, 5th edition

课程评估 ASSESSMENT

19.	评估形式 **Type of Assessment**	评估时间 **Time**	占考试总成绩百分比 **% of final score**	违纪处罚 **Penalty**	备注 **Notes**

出勤 **Attendance**				
课堂表现 **Class Performance**				
小测验 **Quiz**				
课程项目 **Projects**				
平时作业 **Assignments**		40%		作业、程序和报告 Assignments, programs and reports.
期中考试 **Mid-Term Test**		30%		闭卷考试 Unseen exam
期末考试 **Final Exam**		30%		闭卷考试 Unseen exam
期末报告 **Final Presentation**				
其它（可根据需要改写以上评估方式） **Others (The above may be modified as necessary)**				

20. 记分方式 **GRADING SYSTEM**

☑ A. 十三级等级制 **Letter Grading**
☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

课程审批 REVIEW AND APPROVAL

21. **本课程设置已经过以下责任人/委员会审议通过**
This Course has been approved by the following person or committee of authority