课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	**课程名称 Course Title**	**模拟集成电路版图设计 Analog IC layout design**
2.	**授课院系 Originating Department**	电子与电气工程系 Dept. of Electrical and Electronic Engineering
3.	**课程编号 Course Code**	EE339
4.	**课程学分 Credit Value**	1
5.	**课程类别 Course Type**	专业选修课 Major Elective Courses
6.	**授课学期 Semester**	秋季 Fall
7.	**授课语言 Teaching Language**	中文 Chinese
8.	**授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师） Instructor(s), Affiliation& Contact （For team teaching, please list all instructors）**	蒋苓利，教学工程师，电子与电气工程系，jiangll@sustc.edu.cn Lingli Jiang, Teaching engineer, Department of Electrical & Electronic Engineering, jiangll@sustech.edu.cn
9.	**实验员/助教、所属学系、联系方式 Tutor/TA(s), Contact**	待公布 To be announced
10.	**选课人数限额(可不填) Maximum Enrolment （Optional）**	15

11. 授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
学时数 Credit Hours	0	0	32	0	32

12.	先修课程、其它学习要求 Pre-requisites or Other Academic Requirements	EE304 集成电路设计 Integrated Circuit Design
13.	后续课程、其它学习规划 Courses for which this course is a pre-requisite	No
14.	其它要求修读本课程的学系 Cross-listing Dept.	No

教学大纲及教学日历 SYLLABUS

15. 教学目标 Course Objectives

集成电路版图设计是从集成电路设计到工艺制造的一座必经桥梁，它涉及电路、工艺等半导体基础知识以及设计工具和系统的使用。

本课程的教学目标在于学习集成电路的版图设计，上下连接并融会贯通集成电路设计及基本制造工艺。

通过本课程的学习，使学生掌握集成电路设计涉及的基本 CMOS 工艺以及各种器件的版图设计，包括：无源器件、二极管、双极型晶体管、场效应晶体管。在此基础上进一步学习版图布局布线知识，包括对匹配、噪声、隔离等方面的要求。要求学生能看懂并会设计简单版图。

The analog IC layout is the bridge between IC design and the manufacture process. The goal of this course is to learn the layout design principles and skills. With this course, the students can learn the layout of various devices in the basic CMOS process, including passive devices, diodes, bipolar transistors, and field effect transistors. Based on that, we further learn the placement and routing in layout, including matching, noise and isolation requirements.

16. 预达学习成果 Learning Outcomes

通过本课程的学习，学生应当掌握以下知识：

1.可辨认新工艺中的基本元器件，并根据版图复原器件剖面结构图；

2.可按要求进行器件版图设计，包括无源器件、二极管、双极型晶体管、场效应晶体管等；

3.给定工艺库后，可根据工艺库要求进行简单电路版图设计；

4.电路版图设计中，能综合考虑电路匹配、噪声、隔离等要求，设计出符合要求的完整子电路版图；

Through this course, students should master the following knowledge:

1. The basic components in a new process can be identified, and the sectional profile of the devices can be reconstructed according to the layout.

2. The students can design the device layout as required, including passive devices, diodes, bipolar transistors, field-effect transistors, etc.

3. With a given process library, a simple circuit layout design can be realized according to the requirements of the PDK.

4. In IC layout design, matching, noise and isolation can be fully considered, and a sub-circuit layout can be designed to meet the requirements.

17. 课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）
Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

1-4 学时：集成电路版图设计软件的基本使用方法讲解。包括：软件启动、常用的三十几个快捷键、LSW layer view 操作、layer generation 在版图设计中的应用等。

5-8 学时：集成电路版图基本元器件学习；集成电路制造工艺与版图对应关系的学习；根据器件版图还原器件剖面结构图，并根据还原的剖面结构图分析器件结构。

9-12 学时：集成电路版图设计中 hierarchy 概念；集成电路版图中基本元器件学习；集成电路版图 basic 库的要求和基础 Pcell 构建方法。

13-16 学时：模拟集成电路版图设计中匹配的概念；电流镜、差分对等典型电学结构的版图分析。

17-20 学时：模拟集成电路版图设计中噪声和隔离的概念；认知需隔离的电学结构；掌握版图中隔离的方法。

21-32 学时：根据提供的模拟集成电路，进行子电路版图绘制，该电路为真实的 IC 子电路，需要连续几周约 12 小时完成；在绘制过程中，实时进行指导；对学生所绘制的电路版图进行集体点评和分析。

1-4 hours: The basic use of layout software, includes: software startup, thirty commonly used shortcut keys, LSW layer view operation, layer generation application in layout design, etc.

5-8 hours: Learn the basic layout components in IC; Learn the corresponding relationship between layout and the manufacturing process; The section structure of the device based on layout; The analysis of the device structure according to the profile structure.

9-12 hours: Hierarchy concept in IC layout design; Basic components learning in integrated circuit layout; The requirements for layout basic library and the basic Pcell construction method.

13-16 hours: The concept of matching in analog IC layout design; current mirror and differential comparator in layout.

17-20 hours: The concept of noise and isolation in analog IC layout design; The electrical structure should be isolated0; The way to isolate in the layout.

21-32 hours: According to the circuit provided, design the layout of the sub-circuit, it takes about 12 hours; The layout from the students will be collectively reviewed and analyzed.

18. 教材及其它参考资料 Textbook and Supplementary Readings

The Art of Analog Layout (模拟电路版图的艺术)，ISBN：9787121186745

课程评估 ASSESSMENT

19.

评估形式 Type of Assessment	评估时间 Time	占考试总成绩百分比 % of final score	违纪处罚 Penalty	备注 Notes
出勤 Attendance		10%		
课堂表现 Class Performance		20%		
小测验				

Quiz				
课程项目 Projects		70%		
平时作业 Assignments				
期中考试 Mid-Term Test				
期末考试 Final Exam				
期末报告 Final Presentation				
其它（可根据需要改写以上评估方式） Others (The above may be modified as necessary)				

20. 记分方式 **GRADING SYSTEM**

☑ A. 十三级等级制 **Letter Grading**
☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

课程审批 REVIEW AND APPROVAL

21. **本课程设置已经过以下责任人/委员会审议通过**
This Course has been approved by the following person or committee of authority