南方科技大学 SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

# 课程详述

## COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

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| 1. | **课程名称 Course Title** | 专用集成电路设计技术 Application Specific IC（ASIC）Designs Methodology and Practice |
| 2. | **授课院系 Originating Department** | 电子与电气工程系<br>Department of Electrical and Electronic Engineering |
| 3. | **课程编号 Course Code** | EE338 |
| 4. | **课程学分 Credit Value** | 3 |
| 5. | **课程类别 Course Type** | 专业选修课 Major Elective Courses |
| 6. | **授课学期 Semester** | 春季 Spring |
| 7. | **授课语言 Teaching Language** | 中英双语 English & Chinese |
| 8. | **授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师）Instructor(s), Affiliation& Contact （For team teaching, please list all instructors）** | 叶涛，教授，电子与电气工程系<br>yet@sustc.edu.cn |
| 9. | **实验员/助教、所属学系、联系方式 Tutor/TA(s), Contact** | 待公布 To be announced / |
| 10. | **选课人数限额(可不填) Maximum Enrolment （Optional）** | |

| 11. 授课方式 Delivery Method | 讲授 Lectures | 习题/辅导/讨论 Tutorials | 实验/实习 Lab/Practical | 其它(请具体注明) Other（Please specify） | 总学时 Total |
|---|---|---|---|---|---|
| 学时数 Credit Hours | 32 | | 32 | | 64 |

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| 12. 先修课程、其它学习要求 Pre-requisites or Other Academic Requirements | EE201 模拟电路，EE202 数字电路，EE204,半导体器件导论，EE304 集成电路设计 |
| 13. 后续课程、其它学习规划 Courses for which this course is a pre-requisite | 集成电路设计自动化（Electronic Design Automation for ICs） |
| 14. 其它要求修读本课程的学系 Cross-listing Dept. | |

## 教学大纲及教学日历 SYLLABUS

### 15. 教学目标 Course Objectives

专用集成电路（ASIC）是当今微电子行业的一个重要方向。和通用型 IC 和嵌入式系统相比，ASIC 芯片在功耗，成本以及速度上有着很大的优势。ASIC 芯片有着独特的设计理念和设计流程。ASIC 设计是从算法开始，通过硬件设计描述语言 HDL，和标准单元设计库（Standard Cell Library） 结合，经过逻辑综合和优化（Synthesis），布板图（Floor-plan），定位及布线 （Place and Route），物理及逻辑验证（DRC LVS Verification），时序延时分析（Delay Extraction and Timing Annotation，时序验证（Prime Time），最后形成版图（Mask Tape-out）。ASIC 的设计流程， 结合了当今集成电路的许多关键技术， 是培养集成电路人才不可或缺的重要技能。

Application Specific Integrated Circuits (ASIC) is one of the major IC categories in today's semiconductor industry. Compared with general purpose ICs and embedded systems, ASIC chips demonstrate their advantages in power consumption, silicon area, speed, and return-over-investment (ROI) ratio.

Through this course, the students are expected to learn the contemporary methodologies of ASIC design. Particularly, the course will lead students to start the design from algorithmic concept and Verilog HDL description, followed by design steps such as synthesis, floor-planning, placing and routing, timing extraction and verification, DRC and LVS checking, all the way to timing sign-off and GDS mask tape-out. The course will cover the entre ASIC design flow and train students to use EDA tools to design ICs following industrial standard IC design practice.



### 16. 预达学习成果 Learning Outcomes

经过本课程学习，学生将会掌握工业界基本的集成电路设计方法， 包括：

1） 通过硬件描述语言 Verilog HDL 实现算法

2） 电路的 SPICE 模型以及标准单元库以及在电路设计中的应用。

3） 应用集成电路设计的 EDA 设计流程，经过逻辑综合和优化（Synthesis Compilation），布版图（Floor-planning），定位及布线 （Place and Route），物理及逻辑验证（DRC LVS Verification），时序延时分析（Delay Extraction and Timing Annotation），时序验证（Prime Time），最后形成版图（GDS Mask Tape-out）。

4） 在应用要求及设计指标下的设计优化方法， 包括时序， 功耗， 芯片面积及设计可重构化的设计方法。

Through studying this course, the students are expected to learn the industrial standard IC design practice that include.

1) Algorithmic design realization through Verilog HDL.
2) The basic knowledge of Foundry Spice model and Standard Cell Library and how to use them.
3) The knowledge of using EDA design tools that include synthesis compilation, floor-planning, placing and routing, timing extraction and verification, DRC and LVS checking, Primetime timing sign-off and GDS mask tape-out.

Design methodology under customer constrains and trade-offs such as timing, power consumption, and silicon area and design reusability.

**17. 课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）**
**Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)**

Lectures (32 hours)

(1) HDL-based IC design flow. Design flow concept and introduction, Linux basics and command line scripts. (2 hours)

(2) Introduction to Verilog language. Design and editing with GVIM. (2 hours)

(3) Logic and RTL level simulation and Test-bench design. (2 hours)

(4) Verilog description of circuit structure and behavior. (2 hours)

(5) Verilog description in RTL level design. (2 hours)

(6) Verilog syntax and structure, coding style and coding rules. (2 hours)

(7) Verilog delay model and the use of standard-cell library. (2 hours)

(8) Test-bench design and programming. (2 hours)

(9) Logic synthesis and working with scripts in design flow. Case study of RTL synthesis. (2 hours)

(10) Static timing analysis (STA) introduction with scripts in design flow. Case study of RTL STA. (2 hours)

(11) Placement and routing, power ring design and power ring optimization. (2 hours)

(12) Advanced placement and routing, delay extraction after P&R, STA with P&R. (2 hours)

(13) Logic simulation with post-layout timing analysis, timing extraction and timing report. (2 hours)

(14) Introduction to Formality, design-rule-check (DRC) and layout-vs-schematics (LVS). (2 hours)

(15) Design-for-test (DFT) introduction and design ATPG and JTAG. (2 hours)

(16) Memory design and self-testing structure. (2 hours)

Labs and projects (32 hours)

Lab 1. Work with Linux and GVIM environment, shell scripts programming. (4 hours)

Lab 2. Logic simulation and simulation environment, emphasis on testing vectors and testing setups. (4 hours)

Lab 3. Case study of logic design, emphasis on timing sequence and state machine based designs. (4 hours)

Lab 4. Case study, design and simulation, emphasis on timing analysis and testing environment, testing vectors generation. (4 hours)

Lab 5. Logic synthesis and timing path analysis, emphasis on critical path extraction and optimization. (4 hours)

Lab 6. Placement and routing, its techniques and optimization. (4 hours)

Lab 7. Work with Formality、DRC、LVS, emphasis on front-end and back-end co-analysis. (4 hours)

Lab 8. P&R and design-for-testing (DFT) study, timing sign-off and GDS generation. (4 hours)

理论课内容：(32 个学时）

(1)，基于 HDL 设计流程，熟悉 Linux 基本命令，（2 个学时）

(2)，Verilog 语言介绍，熟悉 GVIM 基本操作，（2 个学时）

(3)，逻辑仿真和 Test-bench 编程，（2 个学时）

(4)，Verilog 电路结构级描述，（2 个学时）

(5)，Verilog 基本介绍，（2 个学时）

(6)，Verilog 高级语法级结构，编码风格介绍，（2 个学时）

(7)，Verilog 延时模型, IC 库介绍，仿真，（2 个学时）

(8), Test-bench 设计和仿真,（2 个学时）

(9), 逻辑综合技术,脚本介绍，现场演示案例，（2 个学时）

(10), 静态时序分析 STA 原理介绍，脚本介绍，现场演示，（2 个学时）

(11), 电路的定位及布线 P&R 介绍, Placement,，Route,电源环等介绍，（2 个学时）

(12), 电路的定位及布线 P&R 介绍,时序延时信息提取, STA 分析，（2 个学时）

(13), 后仿动态时序逻辑仿真，时序信息提取和导入，报告简单分析（实例演示），（2 个学时）

(14), Formality、design-rule-check ( DRC) and layout-vs-schematics (LVS)介绍，（2 个学时）

(15)，Design-for-test (DFT)和 ATPG，JTAG 介绍，（2 个学时）

(16) ,实例储存器介绍，内建测试，（2 个学时）

实验课内容：(32 个学时）

实验 1，熟悉 Linux 环境， GVIM 环境， SHELL 编程训练， Scripts 语言，（4 个学时）

实验 2，逻辑仿真工具环境，重点在于测试环境及测试向量的编写（4 个学时）

实验 3，上机做实例设计题，重点在于时序及 State Machine 的编写及简化（4 个学时）

实验 4，实例实验，设计+仿真，重点在于仿真的逻辑测试环境，以及逻辑的可测试向量的设计（4 个学时）

实验 5，逻辑综合和时序分析，重点在于 critical paths 的分析及时序优化（4 个学时）

实验 6，电路的定位及布线 P&R，重点在于学习优化手段及技巧（4 个学时）

实验 7，Formality、DRC、LVS 尝试， 重点在于电路的前后端的数据综合分析（4 个学时）

实验 8，P&R 或 DFT 实验，结合所学的知识， 形成最终经过验证的版图（4 个学时）

**18. 教材及其它参考资料 Textbook and Supplementary Readings**

"CMOS VLSI Design A Circuits and Systems Perspective" 4th edition by Weste and Harris

"Application-Specific Integrated Circuits" , Michael John Sebastian Smith



## 课程评估 ASSESSMENT

**19.**

| 评估形式 Type of Assessment | 评估时间 Time | 占考试总成绩百分比 % of final score | 违纪处罚 Penalty | 备注 Notes |
|---|---|---|---|---|
| 出勤 Attendance | | | | |
| 课堂表现 Class Performance | | | | |
| 小测验 Quiz | | | | |
| 课程项目 Projects | | 30 | | |
| 平时作业 Assignments | | 20 | | |
| 期中考试 Mid-Term Test | | 0 | | |
| 期末考试 Final Exam | | 20 | | |
| 期末报告 Final Presentation | | 30 | | |

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| 其它（可根据需要改写以上评估方式）<br>**Others (The above may be modified as necessary)** | | | | |

20. 记分方式 **GRADING SYSTEM**

☑ A. 十三级等级制 **Letter Grading**
☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

## 课程审批 REVIEW AND APPROVAL

21. 本课程设置已经过以下责任人/委员会审议通过
**This Course has been approved by the following person or committee of authority**