课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	**课程名称 Course Title**	集成电路设计 Integrated Circuit Design
2.	**授课院系 Originating Department**	电子与电气工程 Electrical and Electronic Engineering
3.	**课程编号 Course Code**	EE304
4.	**课程学分 Credit Value**	3
5.	**课程类别 Course Type**	专业核心课 Major Core Courses
6.	**授课学期 Semester**	春季 Spring
7.	**授课语言 Teaching Language**	中英双语 English & Chinese
8.	**授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师）Instructor(s), Affiliation& Contact （For team teaching, please list all instructors）**	詹陈长，助理教授，电子与电气工程系 第一教学楼 105 室 zhancc@sustech.edu.cn 0755-8801-5480 ZHAN Chenchang, Assistant Professor, Department of Electrical and Electronic Engineering Rm.105, Lecture Hall 1. zhancc@sustech.edu.cn 0755-8801-5480
9.	**实验员/助教、所属学系、联系方式 Tutor/TA(s), Contact**	乔鸿昌，研究生，电子与电气工程系 第一教学楼 207 室 11749190@mail.sustech.edu.cn 0755-8801-5461 QIAO Hongchang, PG Student, Department of Electrical and Electronic Engineering Rm.207, Lecture Hall 1. 11749190@mail.sustech.edu.cn 0755-8801-5461
10.	**选课人数限额(可不填) Maximum Enrolment （Optional）**	

11. 授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
学时数 Credit Hours	16	0	64		80

12. 先修课程、其它学习要求 Pre-requisites or Other Academic Requirements	EE202 数字电路 EE204 半导体器件导论 EE202 Digital Circuits EE204 Introduction to Semiconductor Devices
13. 后续课程、其它学习规划 Courses for which this course is a pre-requisite	无 NA
14. 其它要求修读本课程的学系 Cross-listing Dept.	无 NA

教学大纲及教学日历 SYLLABUS

15. 教学目标 Course Objectives

介绍 CMOS 超大规模集成电路设计相关概念、方法，包括 MOS 器件及其建模、CMOS 工艺和版图设计规则、静态和动态逻辑门电路原理和设计考虑。同时，采用业界标准的设计工具培养集成电路设计实践能力。

To introduce the basic concepts and methodologies in modern CMOS VLSI design. These include the MOS devices and modelling, CMOS process and design rules, behaviours and design considerations of both the static and dynamic logic gates. Use the industry standard EDA tools to guide the students through designing real-world integrated circuits.

16. 预达学习成果 Learning Outcomes

通过本课程学习，学生将熟悉一些与现代 CMOS 超大规模集成电路设计相关的概念和方法，理解 MOS 管的工作原理与数学模型，学会使用 MOS 管设计数字逻辑门电路，理解 CMOS 超大规模集成电路基本工艺、版图设计、封装选择，理解针对包括速度、功耗和面积等在内的各种关键指标的设计折中，学会使用业界标准的电子设计自动化工具进行集成电路的设计和验证。

After completing this course, students will be able to

1) Get familiar with the basic concepts and methods related to modern CMOS VLSI circuits.
2) Understand the MOS transistor operation principle and mathematical modelling.
3) Use MOS transistors to design digital logic gates.
4) Understand the basic CMOS VLSI process technology, layout considerations and packaging options.
5) Understand the design trade-offs among speed, power and area consumptions.
6) Use the industry-standard EDA tools to design and verify an integrated circuit.

17. 课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）

Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

Chapter 1. Introduction to CMOS VLSI Design: Historical development of VLSI design; Design challenges, approach and flow; Circuit and system representation; Standard cell versus full custom; Hierarchical design.

Chapter 2. MOS Transistor Theory Part I—Basic Operation and Modelling: Basic introduction to the MOS transistor, MOS structure, Different modes of MOS function, MOS first order modelling.

Chapter 3. MOS Transistor Theory Part II—Second-Order Modelling: Second order effects in MOSFET--Body effect, Channel-length modulation, Subthreshold conduction; Short-channel effects--Threshold voltage variation, Mobility degradation with vertical field, Velocity saturation, Hot carrier effects.

Chapter 4. CMOS Combinational Logic Circuit Design: General recipe for complex combinational circuits; Transistor sizing in combinational circuits; Different logic styles; Layout designs of CMOS combinational functions--Euler-path diagram, Transistor ordering for lower parasitic capacitance and reduced silicon area, Standard cell based layout design approach.

Chapter 5. CMOS Technology, Layout and Packaging: Semiconductor properties; Fabrication process: making transistors and wires; Common fabrication process errors; Design rules; CMOS layout design considerations; IC packaging.

Chapter 6. CMOS Inverter DC Characteristics: CMOS inverter reexamination; Static behavior of a CMOS inverter--Voltage Transfer Curve (VTC), Noise margins, βn /βp ratio.

Chapter 7. CMOS Timing and Dynamic Circuit Characteristics: Dynamic behavior of CMOS inverter--RC characterization of CMOS circuits, □Fall time, rise time and delay analysis; Delay of complex gates--Elmore delay model; Driving large loads; □Power consumption--Dynamic power consumption, Short-circuit current, Leakage.

Chapter 8. Advanced CMOS Logic Circuit Design: High speed design considerations; Review of static CMOS gates--Complementary logic, Ratioed logic, Pass transistor logic; Dynamic CMOS logic--Basic principles and examples, Properties of dynamic logic gates, Performance and limitations; Domino logic--General operation and properties, Performance and Limitations.

18. 教材及其它参考资料 Textbook and Supplementary Readings

指定教材: Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education Asia Limited, 2003.

推荐参考资料: Neil H. E. Weste and David M. Harris, CMOS VLSI Design, 4th Edition, Pearson Education Asia Limited, 2010.

Required: Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education Asia Limited, 2003.

Recommended: Neil H. E. Weste and David M. Harris, CMOS VLSI Design, 4th Edition, Pearson Education Asia Limited, 2010.

课程评估 ASSESSMENT

19.

评估形式 Type of Assessment	评估时间 Time	占考试总成绩百分比 % of final score	违纪处罚 Penalty	备注 Notes
出勤 Attendance		10%		
课堂表现 Class Performance		10%		
小测验 Quiz				
课程项目 Projects		50%		
平时作业		10%		

Assignments				
期中考试 Mid-Term Test		20%		
期末考试 Final Exam				
期末报告 Final Presentation				
其它（可根据需要改写以上评估方式） Others (The above may be modified as necessary)				

20. 记分方式 **GRADING SYSTEM**

☑ A. 十三级等级制 **Letter Grading**
☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

课程审批 REVIEW AND APPROVAL

21. 本课程设置已经过以下责任人/委员会审议通过
This Course has been approved by the following person or committee of authority