# 课程大纲
# COURSE SYLLABUS

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| **1.** | **课程代码/名称**<br>**Course Code/Title** | 高阶 CMOS 超大规模集成电路设计 Advanced CMOS VLSI Design |
| **2.** | **课程性质**<br>**Compulsory/Elective** | 专业核心课<br>Major Core Courses |
| **3.** | **课程学分/学时**<br>**Course Credit/Hours** | 3/64 |
| **4.** | **授课语言**<br>**Teaching Language** | 中英<br>Chinese&English |
| **5.** | **授课教师**<br>**Instructor(s)** | 安丰伟 An Fengwei |
| **6.** | **先修要求**<br>**Pre-requisites** | EE202 数字电路, EE204 半导体器件导论<br>EE202 Digital circuit; Introduction of semiconductor devices |
| **7.** | **教学目标**<br>**Course Objectives** | |
| | 本课程介绍高阶 CMOS 超大规模集成电路设计的概念和设计方法，包括随机存储存取器（SRAM）涉及到的复杂组合逻辑电路和时序电路等的电路图设计与仿真、版图设计以及利用此 SRAM 设计一个 RISC CPU 包括程序计数器、指令译码器、指令执行模块、有限状态机等。本课程可以培养学生在以下方面的能力：全定制和半定制电路原理图设计和仿真、版图设计和版图后仿真。<br>This course introduces the concepts and design methods for advanced CMOS VLSI design, including schematic design, simulation and layout for complicated combinatorial logic circuits and sequential circuits involved in the static random access memory (SRAM). Design a RISC CPU includes a program counter, an instruction decoder, an instruction execution module, a finite state machine, and the data/instruction memory (Full custom designed SRAM). This course develops students' skills in full-custom and semi-custom schematic design and simulation, layout design and post-layout simulation. | |
| **8.** | **教学方法**<br>**Teaching Methods** | |
| | 讲授 Lectures, 习题/辅导/讨论 Tutorials, 实验/实习 Lab/Practical | |
| **9.** | **教学内容**<br>**Course Contents** | |
| | **Section 1** | Introduction to Advanced CMOS Logic Circuit Design: CMOS Technology, Layout and Packaging. （第 1 课：高阶 CMOS 超大规模集成电路设计介绍；2 学时） |
| | **Section 2** | Delay, Power, Robustness of the CMOS Circuit (第 2 课: CMOS 电路的延迟、功耗、可靠性) |
| | **Section 3** | CMOS Combinational Logic Circuit Design: Encoder, decoder, multiplier.（第 3 课：CMOS 组合逻辑电路设计；2 学时） |
| | **Section 4** | CMOS Sequential Circuit design: Latches and D-Flip-Flop （第 4 课：CMOS 时序逻辑电路；2 学时） |
| | **Section 5** | SRAM design (1): SRAM bit cell, Row Circuitry, Column Circuitry,（第 5 课：SRAM 设计 （1）；2 学时） |
| | **Section 6** | SRAM design (2): Multi-ported SRAM and Register Files, Area, Delay, and |

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| | | Power of SRAMs （第 16 课：SRAM 设计（2））|
| | **Section 7** | ALU design for the RISC CPU: Verilog HDL modeling for ALU design （第 7 课：精简指令集 CPU 的算术逻辑单元设计） |
| | **Section 8** | State machine design for the RISC CPU （第 8 课：精简指令集 CPU 状态机设计） |
| | **Labs** | Lab 1. Linux Setup, Schematic Design and Simulation: Linux setup and Cadence basic, Schematic entry and simulation with Analog Design Environment, Hierarchical Schematic Design. （实验 1：Linux 系统设置、电路原理图设计与仿真；2 学时）<br>Lab 2. Schematic Design and Simulation for SRAM design: Schematic design and HSpice simulation（实验 2：版图设计与验证；20 学时）<br>Lab 3. Layout Design and Verifications for SRAM design: Layout design and design rule check (DRC), Layout versus schematic (LVS). （实验 2：版图设计与验证；20 学时）<br>Lab 3. Post-Layout Simulation for SRAM: Parasitic extraction, Post-Layout Simulation（实验 3：版图后仿真；2 学时）<br>Lab 4. Verilog HDL design with the designed SRAM for RISC CPU: Simulation, synthesis, place and route for RISC CPU （实验 4：精简指令集 CPU 设计；20 学时） |
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**10. 课程考核**
**Course Assessment**

请再此注明：①考查/考试；②分数构成。
考查 Checking

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| 课堂报告 | Presentation | 40% |
| 期中项目 | Mid-Term Project | 18% |
| 期末项目 | Final Project | 42% |

**11. 教材及其它参考资料**
**Textbook and Supplementary Readings**

指定教材: Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education Asia Limited, 2003.

推荐参考资料: Neil H. E. Weste and David M. Harris, CMOS VLSI Design, 4th Edition, Pearson Education Asia Limited, 2010.

Required: Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education Asia Limited, 2003.

Recommended: Neil H. E. Weste and David M. Harris, CMOS VLSI Design, 4th Edition, Pearson Education Asia Limited, 2010.