课程详述

COURSE SPECIFICATION

以下课程信息可能根据实际授课需要或在课程检讨之后产生变动。如对课程有任何疑问，请联系授课教师。

The course information as follows may be subject to change, either during the session because of unforeseen circumstances, or following review of the course at the end of the session. Queries about the course should be directed to the course instructor.

1.	**课程名称 Course Title**	集成电路基础 II Fundamentals of Integrated Circuit II
2.	**授课院系** **Originating Department**	深港微电子学院 School of Microelectronics
3.	**课程编号** **Course Code**	SME202
4.	**课程学分 Credit Value**	4
5.	**课程类别** **Course Type**	专业选修课 Major Elective Courses
6.	**授课学期** **Semester**	春季及秋季 Spring and Fall
7.	**授课语言** **Teaching Language**	英语 English/中英双语 English & Chinese
8.	**授课教师、所属学系、联系方式（如属团队授课，请列明其他授课教师）** **Instructor(s), Affiliation& Contact** **（For team teaching, please list all instructors）**	汪 飞，副教授，深港微电子学院 Fei Wang, Associate Professor, School of Microelectronics, Email: wangf@sustech.edu.cn 王师惟，助理教授，深港微电子学院 Shiwei Wang，Asisstant Professor，School of Microelectronics.
9.	**实验员/助教、所属学系、联系方式** **Tutor/TA(s), Contact**	待公布 To be announced
10.	**选课人数限额(可不填)** **Maximum Enrolment（Optional）**	

11.	授课方式 Delivery Method	讲授 Lectures	习题/辅导/讨论 Tutorials	实验/实习 Lab/Practical	其它(请具体注明) Other（Please specify）	总学时 Total
	学时数 Credit Hours	48		32		80

12.	先修课程、其它学习要求 Pre-requisites or Other Academic Requirements	SME102 微电子及集成电路基础概论 Fundamentals of Microelectronics and Integrated Circuit
13.	后续课程、其它学习规划 Courses for which this course is a pre-requisite	
14.	其它要求修读本课程的学系 Cross-listing Dept.	

教学大纲及教学日历 SYLLABUS

15. 教学目标 Course Objectives

本课程（集成电路基础 II，SME202）与集成电路基础 I（SME201）是微电子专业本科生的两门专业基础课，其讲授内容是深港微电子学院先导课程 SME102 分别在模拟和数字集成电路设计两个重要基础方向的延伸和进阶。本课程主要任务是让学生掌握大规模 CMOS 集成电路设计以及 Verilog HDL 硬件描述语言的基本概念、基本原理、基本分析与设计方法；培养学生使用 Verilog HDL 描述 CMOS 集成电路的逻辑功能的基本技能，培养学生根据具体问题，分析功能需求，设计集成电路的基本能力，为以后从事集成电路设计领域的工程技术工作、科学研究工作以及开拓新技术领域奠定基础。本科介绍以下 5 大方面的知识：

1. CMOS 集成电路基础
2. 动态/静态 CMOS 集成电路
3. 同步时序电路的分析和设计
4. Verilog HDL 层次建模、数据流建模、行为级建模
5. 时序和延迟基础知识以及使用 Verilog HDL 进行逻辑综合

This course (Fundamentals of Integrated Circuit II, SME202) and Fundamentals of Integrated Circuit I (SME201) together are two major foundational courses for the undergraduates majoring in microelectronics. They are the extensions of SME102 in two important aspects—analog and digital integrated circuit design. The main task of this course is to let students understand the basic concepts, basic principles, basic analysis and design methods of large-scale CMOS integrated circuit design and Verilog HDL hardware description language; train students to use Verilog HDL to design a CMOS integrated circuit. According to specific problems, students analyze the functional specifications and design the integrated circuits. This will lay the foundation for future engineering and scientific research in the field of integrated circuit design. This course introduces the following 5 major areas of knowledge:

1. CMOS integrated circuit foundation
2. Dynamic/Static CMOS IC
3. Analysis and design of synchronous sequential circuit
4. Verilog HDL level modeling, data flow modeling, behavioral level modeling
5. Basic knowledge of timing delay and logic synthesis using Verilog HDL

16. 预达学习成果 Learning Outcomes

本课程通过理论课教学，使学生掌握

1.CMOS 集成电路的基本分析思路与设计方法，

2.CMOS 集成电路基础、门电路、组合逻辑电路、时序逻辑电路的基本概念、原理、分析与设计方法；

3.Verilog HDL 硬件编程语言的语法、建模方法、仿真方法、综合方法。

课程实验是该课程的主要实践教学环节之一，其主要目的是

4.训练学生如何分析问题，通过针对问题建模进行逻辑电路与系统设计的基本实验技能训练，巩固和加深所学到的理论知识。

5.培养学生运用基本理论分析、处理实际问题的能力；掌握 CMOS 集成电路的计算机辅助设计和仿真分析的方法，学会分析 CMOS 集成电路参数及性能分析，培养基本的 CMOS 集成电路与系统设计能力。
6.通过实践教学环节不仅要培养学生基本动手能力，还要培养学生良好的科学素养。
This course enables students to understand
1. Basic analysis ideas and design methods of CMOS integrated circuits,
2.Basic concepts, principles, analysis and design methods of CMOS integrated circuit foundation, gate circuit, combinational logic circuit, sequential logic circuit;
3.The syntax, modeling method, simulation method and synthesis method of Verilog HDL hardware programming language.
Course experiment is one of the main practical teaching links of the course, and its main purpose is
1.Train students how to analyze problems, and consolidate and deepen the theoretical knowledge they have learned through basic experimental skills training of logic circuits and system design for problem modeling.
2.Cultivate students' ability to use basic theories to analyze and deal with practical problems; master the computer-aided design and simulation analysis methods of CMOS integrated circuits, learn to analyze CMOS integrated circuit parameters and performance analysis, and cultivate basic CMOS integrated circuit and system design capabilities.
3.Through the practice teaching link, not only the basic practical ability of students should be cultivated, but also the good scientific literacy of students should be cultivated.

17. 课程内容及教学日历 （如授课语言以英文为主，则课程内容介绍可以用英文；如团队教学或模块教学，教学日历须注明主讲人）
Course Contents (in Parts/Chapters/Sections/Weeks. Please notify name of instructor for course section(s), if this is a team teaching or module course.)

本课程涵盖集成电路的基础知识、集成电路的基本 CMOS 逻辑门电路的相关内容、以及 Verilog HDL 硬件描述语言，介绍以下 5 大方面的知识：

1. CMOS 集成电路的基础知识

2. CMOS 集成电路逻辑门电路：组合逻辑和时序逻辑电路

3. 同步时序电路的分析和设计

4. Verilog HDL 层次建模、数据流建模、行为级建模

5. 时序和延迟基础知识以及使用 Verilog HDL 进行逻辑综合

重点内容是 CMOS 集成电路、常用组合逻辑电路和常用时序逻辑电路。难点是时序逻辑电路的分析和设计。本课程由理论教学和课程实验两部分组成，其中理论授课学时为 48 学时，课程实验学时为 32 学时

本课程理论课的教学日历如下：

课程内容	学时分配	教学要求、重点与难点
第一章 CMOS 集成电路基础 CMOS 集成电路工艺与器件 逻辑函数	8	晶体管与逻辑代数
第二章 CMOS 反相器 静态 CMOS 反相器 CMOS 反相器稳定性评估 CMOS 反相器动态特性 CMOS 反相器功耗、能量、以及能量延时	6	工艺尺寸缩小对反相器衡量指标的影响
第三章 CMOS 组合逻辑电路 常用中规模组合逻辑电路——编码器、译码器、选择器、加法器、比较器、数据选择器等 静态 CMOS 设计 动态 CMOS 设计	6	如何设计复杂的 CMOS 组合逻辑电路

第四章 边沿触发器与锁存器 静态锁存器和寄存器 动态锁存器和寄存器 其他寄存器类型	6	常用寄存器的性能指标
第五章 时序逻辑电路 时序逻辑电路的结构、功能特点与分类 同步时序逻辑电路分析 时序逻辑电路的分析方法 异步时序逻辑电路分析 有限状态机设计	6	流水线：优化时序电路的一种方法
第六章 Verilog HDL 系统综述 1）硬件描述语言的意义 2）Verilog HDL 的优点 3）硬件描述语言的发展趋势	2	Verilog HDL 与 VHDL 的区别
第七章 层次建模 设计方法学 四位脉动进位计数器 模块实例化 逻辑仿真 模块和端口 门级建模	6	CMOS 大规模集成电路的设计方法
第八章 数据流和行为级建模 赋值语句 延迟、表达式、操作符和操作数 结构化过程语句 时序控制语句 多路分支语句 顺序块和并行块 任务和函数 逻辑综合	6	有限状态机的设计方法
习题复习	2	

本课程实验课的教学日历如下：

实验项目	学时分配	实验要求
实验环境	2	熟悉 FPGA 的编译环境
组合 CMOS 集成电路设计	2	（1）反相器、组合逻辑设计和仿真 （2）全加器电路的设计和仿真； （3）译码器电路的设计和仿真； （4）乘法器电路的设计和仿真。
时序 CMOS 集成电路设计	4	（1）边沿 D 触发器设计及仿真； （2）移位寄存器功能设计及应用； （3）各种计数器原理测试及设计。
大规模集成电路设计	4	（1）掌握卷积中常用乘加器设计及仿真 （2）掌握流水线乘加器设计及仿真
课程项目	20	项目名称：低延迟乘加器设计 项目目的：设计一个使用定制化加法器的低延迟的乘加器。

This course covers the basic knowledge of integrated circuits, the related content of the basic CMOS logic gate circuits of integrated circuits, and the Verilog HDL hardware description language, and introduces the following five major aspects of knowledge:

1. Basic knowledge of CMOS integrated circuits

2. CMOS integrated circuit logic gate circuit: combinational logic and sequential logic circuit

3. Analysis and design of synchronous sequential circuit

4. Verilog HDL level modeling, data flow modeling, behavioral level modeling

5. Basic knowledge of timing and delay and logic synthesis using Verilog HDL

The focus is on CMOS integrated circuits, commonly used combinational logic circuits and commonly used sequential logic circuits. The difficulty is the analysis and design of sequential logic circuits. This course is composed of two parts: theory teaching and course experiment. The theoretical teaching hours are 48 hours, and the course experiment hours are 32 hours.

The teaching calendar of the theoretical lessons of this course is as follows:

Course content	Class allocation	Teaching requirements, key points and difficulties
Chapter 1 CMOS Integrated Circuit Basics 1) CMOS integrated circuit technology and devices 2) Logic functions 8 Transistors and logic algebra	**8**	Transistors and logic algebra
Chapter 2 CMOS Inverter 1) Static CMOS inverter 2) Evaluation of CMOS inverter stability 3) CMOS inverter dynamic characteristics 4) CMOS inverter power consumption, energy, and energy delay	**6**	The impact of shrinking process size on inverter metrics
Chapter 3 CMOS Combinational Logic Circuit 1) Commonly used medium-scale combinational logic circuits-encoders, decoders, selectors, adders, comparators, data selectors, etc. 2) Static CMOS design 3) Dynamic CMOS design	**6**	How to design complex CMOS combinational logic circuits
Chapter 4 Edge trigger and latch 1) Static latches and registers 2) Dynamic latches and registers 3) Other register types	**6**	Performance indicators of commonly used registers
Chapter 5 Sequential Logic Circuit 1) The structure, function characteristics and classification of sequential logic circuits 2) Analysis of synchronous sequential logic circuit 3) Analysis method of sequential logic circuit 4) Analysis of asynchronous sequential logic circuit 5) Finite state machine design	**6**	Pipeline: A way to optimize sequential circuits
Chapter 6 Overview of Verilog HDL System 1) The meaning of hardware description language 2) Advantages of Verilog HDL 3) The development trend of hardware description language	**2**	The difference between Verilog HDL and VHDL
Chapter 7 Hierarchical Modeling 1) Design methodology 2) Four-digit pulse carry counter 3) Module instantiation 4) Logic simulation 5) Modules and ports 6) Gate-level modeling	**6**	Design Method of CMOS Large Scale Integrated Circuit

Chapter 8 Data Flow and Behavioral Modeling 1) Assignment statement 2) Delays, expressions, operators and operands 3) Structured procedure statement 4) Timing control statement 5) Multiple branch statements 6) Sequential block and parallel block 7) Tasks and functions 8) Logic synthesis	**6**	Design method of finite state machine
Exercise review	**2**	

The teaching calendar of the Lab of this course is as follows:

Lab iterms	**Class allocation**	**Teaching requirements, key points and difficulties**
lab environment	2	Familiar with FPGA compilation environment
Combined CMOS integrated circuit design	2	(1) Inverter, combinational logic design and simulation (2) Design and simulation of full adder circuit; (3) Design and simulation of decoder circuit; (4) Design and simulation of multiplier circuit.
Timing CMOS integrated circuit design	4	(1) Design and simulation of edge D flip-flop; (2) Functional design and application of shift register; (3) Test and design of various counter principles.
Large-scale integrated circuit design	4	(1) Master the design and simulation of multipliers and adders commonly used in convolution (2) Master the design and simulation of pipeline multiplier and adder
Course Project	20	Project Title: Design of Low Latency Multiplier and Adder Project objective: Design a low-latency multiplier and adder using a customized adder.

18. 教材及其它参考资料 Textbook and Supplementary Readings

教材 Textbooks:

1.Microelectronic Circuits,8th Edition, Adel S Sedra&Kenneth C Smith &Tony Chan Carusone&Vincent Gaudet, Oxford University Press, 2019 年 2 月.

2. 数字电子技术基础（第六版），阎石主编，高等教育出版社，2016 年 4 月.

3. 数字集成电路：电路、系统与设计（第二版），Rabaey 编，电子工业出版社，2004 年 10 月.

参考书 References:

1.数字系统与逻辑设计，刘宝琴主编，清华大学出版社，2004.

2. Verilog 数字设计与综合（第二版），帕尔尼卡编，电子工业出版社，2004 年 11 月.

3. Digital Logic Circuit Analysis and Design, Victor P. Nelson,清华大学出版社, 1997.

4. Verilog® HDL. 2nd ed. Pearson Education, Palnitkar, Samir. 2003.

5 .Digital Electronics - A Practical Approach With VHDL 9/e ,W. Kleitz, Pearson, 2012.

课程评估 ASSESSMENT

19.

评估形式 Type of Assessment	**评估时间 Time**	**占考试总成绩百分比 % of final score**	**违纪处罚 Penalty**	**备注 Notes**
出勤 Attendance				
课堂表现 Class Performance		5		

小测验 **Quiz**		20		
课程项目 **Projects**				
平时作业 **Assignments**		15		
期中考试 **Mid-Term Test**		20		
期末考试 **Final Exam**		40		
期末报告 **Final Presentation**				
其它（可根据需要改写以上评估方式） **Others (The above may be modified as necessary)**				

20. 记分方式 **GRADING SYSTEM**

☑ A. 十三级等级制 **Letter Grading**
☐ B. 二级记分制（通过/不通过） **Pass/Fail Grading**

课程审批 REVIEW AND APPROVAL

21. 本课程设置已经过以下责任人/委员会审议通过
This Course has been approved by the following person or committee of authority